## REMARKS

Reconsideration is requested.

Claim 258 has been amended to obviate the claim objection.

Claims 253-284 are rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claims 1-30 of U.S. Patent No. 6,466,634 B1. A Terminal Disclaimer is enclosed to obviate this rejection.

Claim 253 is rejected under 35 U.S.C. § 102 as being anticipated by U.S. Patent No. 5,121,407 to Partyka.

Claim 253-255, 260, 263, 266-269, 272-273 and 280-282 are rejected under 35 U.S.C. §103(a) as being unpatentable over Partyka (U.S. Patent No. 5,121,407) as applied above and Sutardja (U.S. Patent No. 5,576,647).

Claim 253, as presently written, recites a "voltage controlled oscillator configured to multiply the frequency of the digital clock signal by a predetermined multiple" together with "divider circuitry being configured to divide by the predetermined multiple."

The Partyka et al. reference fails to teach or suggest a voltage controlled oscillator configured to multiply the frequency of the digital clock signal by a predetermined multiple combined with divider circuitry configured to divide by the same predetermined multiple. There is no teaching or suggestion in the Partyka et al. reference that the divider should divide by the same multiple that the voltage controlled oscillator uses to multiply the

frequency of the digital clock signal. There is no disclosure in the Partyka et al. reference of using the voltage controlled oscillator 110 to multiply the frequency of the digital clock signal by a predetermined multiple in combination with using divider circuitry to divide by the same predetermined multiple. Instead, in the Partyka et al. reference, the divisor of divider 122 is changed from M to M+1 to change the frequency of the oscillator during a continuous wave period. According to Partyka et al., transmission of data twice on two separate frequencies differing by odd multiples of N/2*Ts (where N is a number of sequences and Ts is a period of a pseudo noise sequence) causes no CW jamming signal spectral components being present in the receiver pass band to corrupt the message on at least one of the two frequencies to guarantee that the message will be properly received.

The Sutardja et al. reference fails to cure the deficiency of Partyka et al.

Therefore, claim 253 is allowable.

As claims 254-258 depend on claim 253, they too are allowable.

Claim 260, as amended, recites a CMOS transmitter configured to receive a digital clock signal, the transmitter comprising a phase locked loop including a voltage controlled oscillator configured to multiply the frequency of the digital clock signal by a predetermined multiple, control circuitry coupled to the phase locked loop to maintain a desired frequency, the voltage controlled oscillator having a plurality of outputs that, in operation, are

angularly spaced apart with respect to phase, the phase locked loop having an output providing a transmitter carrier; divider circuitry having an input coupled to at least one of the outputs of the voltage controlled oscillator, the divider circuitry being configured to divide by the predetermined multiple and having an output coupled to the control circuitry; and a modulator coupled to the phase locked loop and configured to use the transmitter carrier.

The Partyka et al. reference fails to teach or suggest a voltage controlled oscillator configured to multiply the frequency of the digital clock signal by a predetermined multiple combined with divider circuitry configured to divide by the same predetermined multiple.

The Sutardja reference fails to cure the deficiency of the Partyka et al. reference. Therefore, claim 260 is allowable.

As claims 261-265 depend on claim 260, they too are allowable.

Claim 266 recites an integrated circuit including carrier circuitry configured to provide a carrier for wireless communications, the carrier circuitry being configured to receive a digital clock signal, the carrier circuitry being defined by CMOS circuit elements, the carrier circuitry comprising a phase locked loop including a voltage controlled oscillator configured to multiply the frequency of the digital clock signal by a predetermined multiple, control circuitry configured compare the frequency and phase of the digital clock signal to a second signal and to issue pump up or pump down signals in response to the comparison, and a charge pump coupled to the control

circuitry and configured to maintain a desired frequency in response to the pump up and pump down signals, the charge pump being configured to receive the pump up and pump down signals and produce an output having a voltage that varies in response to the pump up and pump down signals, the voltage controlled oscillator having an output, the phase locked loop having an output configured to provide a transmitter carrier; and divider circuitry having an input coupled to the output of the voltage controlled oscillator, the divider circuitry being configured to divide by the predetermined multiple and having an output coupled to the control circuitry.

The Partyka et al. reference fails to teach or suggest a voltage controlled oscillator configured to multiply the frequency of the digital clock signal by a predetermined multiple combined with divider circuitry configured to divide by the same predetermined multiple.

The Sutardja reference fails to cure the deficiency of the Partyka et al. reference. Therefore, claim 266 is allowable.

As claims 272-279 depend on claim 266, they too are allowable.

Claim 280 recites a communications system including a transmitter integrated circuit for wireless communications, the transmitter integrated circuit being configured to receive a digital clock signal, the transmitter integrated circuit being defined by CMOS circuit elements and comprising a phase locked loop including a voltage controlled oscillator configured to multiply the frequency of the digital clock signal by a predetermined multiple,

control circuitry configured to receive the digital clock signal and to compare the frequency and phase of the digital clock signal with a second signal and to issue pump up or pump down signals in response to the comparison, and a charge pump coupled to the control circuitry and the voltage controlled oscillator to maintain a desired frequency in response to the pump up and pump down signals, the voltage controlled oscillator having a plurality of outputs that are angularly spaced apart with respect to phase, the phase locked loop having an output providing a transmitter carrier; divider circuitry having an input coupled to at least at least one of the outputs of the voltage controlled oscillator, the divider circuitry dividing by the predetermined multiple and having an output defining the second signal coupled to the control circuitry; and a modulator coupled to the voltage controlled oscillator.

The Partyka et al. reference fails to teach or suggest a voltage controlled oscillator configured to multiply the frequency of the digital clock signal by a predetermined multiple combined with divider circuitry configured to divide by the same predetermined multiple.

The Sutardja reference fails to cure the deficiency of the Partyka et al. reference. Therefore, claim 280 is allowable.

As claims 281-284 depend on claim 280, they too are allowable.

In view of the foregoing, allowance of claims 253-284 is requested. The Examiner is requested to phone the undersigned in the event that the next Office Action is one other that a Notice of Allowance. The undersigned is available for telephone consultation at any time during normal business hours (Pacific Time Zone).

Respectfully submitted,

Dated: June 28, 2004 By: _____

Deepak Malhotra
Reg. No. 33,560